# MC14020B

# 14-Bit Binary Counter

The MC14020B 14−stage binary counter is constructed with MOS P−Channel and N−Channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple−carry binary counter. The device advances the count on the negative−going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency−dividing circuits.

### Features

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- Pin−for−Pin Replacement for CD4020B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

**MAXIMUM RATINGS** (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage Range | −0.5 to +18.0 | V |
| $V_{in}$, $V_{out}$ | Input or Output Voltage Range (DC or Transient) | −0.5 to $V_{DD}$ + 0.5 | V |
| $I_{in}$, $I_{out}$ | Input or Output Current (DC or Transient) per Pin | ±10 | mA |
| $P_D$ | Power Dissipation, per Package (Note 1) | 500 | mW |
| $T_A$ | Ambient Temperature Range | −55 to +125 | °C |
| $T_{stg}$ | Storage Temperature Range | −65 to +150 | °C |
| $T_L$ | Lead Temperature (8−Second Soldering) | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Packages: –7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.

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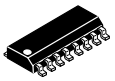
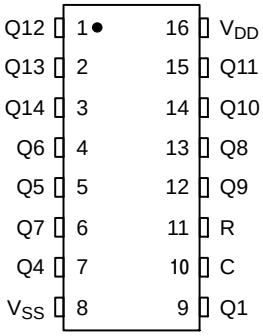


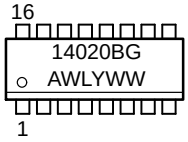
**SOIC−16**
**D SUFFIX**
**CASE 751B**

**TSSOP−16**
**DT SUFFIX**
**CASE 948F**

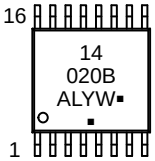
**PIN ASSIGNMENT**




**MARKING DIAGRAMS**




**SOIC−16**




**TSSOP−16**

| | |
|---|---|
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| YY, Y | = Year |
| WW, W | = Work Week |
| G or ▪ | = Pb−Free Indicator |

(Note: Microdot may be in either location)

**ORDERING INFORMATION**

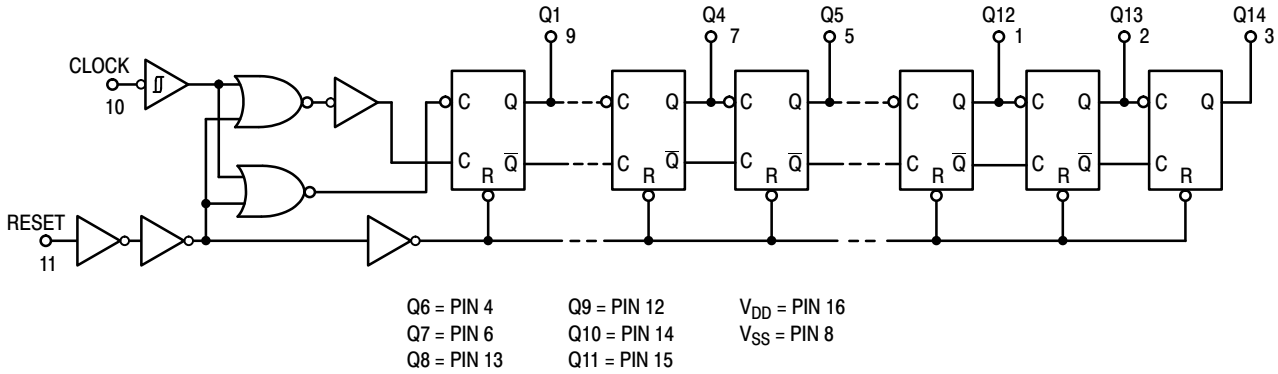
See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

**TRUTH TABLE**

| Clock | Reset | Output State |
|---|---|---|
| ⌐ | 0 | No Change |
| ¬ | 0 | Advance to Next State |
| X | 1 | All Outputs are Low |

X = Don't Care

**LOGIC DIAGRAM**




**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| MC14020BDG | SOIC−16<br>(Pb−Free) | 48 Units / Rail |
| MC14020BDR2G | SOIC−16<br>(Pb−Free) | 2500 Units / Tape & Reel |
| NLV14020BDR2G* | SOIC−16<br>(Pb−Free) | 2500 Units / Tape & Reel |
| MC14020BDTG | TSSOP−16<br>(Pb−Free) | 96 Units / Rail |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$)

| Characteristic | Symbol | $V_{DD}$ Vdc | −55°C Min | −55°C Max | 25°C Min | 25°C Typ (Note 2) | 25°C Max | 125°C Min | 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage “0” Level | $V_{OL}$ | 5.0 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | Vdc |
| $V_{in}$ = $V_{DD}$ or 0 | | 10 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | |
| | | 15 | – | 0.05 | – | 0 | 0.05 | – | 0.05 | |
| “1” Level | $V_{OH}$ | 5.0 | 4.95 | – | 4.95 | 5.0 | – | 4.95 | – | Vdc |
| $V_{in}$ = 0 or $V_{DD}$ | | 10 | 9.95 | – | 9.95 | 10 | – | 9.95 | – | |
| | | 15 | 14.95 | – | 14.95 | 15 | – | 14.95 | – | |
| Input Voltage “0” Level | $V_{IL}$ | | | | | | | | | Vdc |
| ($V_O$ = 4.5 or 0.5 Vdc) | | 5.0 | – | 1.5 | – | 2.25 | 1.5 | – | 1.5 | |
| ($V_O$ = 9.0 or 1.0 Vdc) | | 10 | – | 3.0 | – | 4.50 | 3.0 | – | 3.0 | |
| ($V_O$ = 13.5 or 1.5 Vdc) | | 15 | – | 4.0 | – | 6.75 | 4.0 | – | 4.0 | |
| “1” Level | $V_{IH}$ | | | | | | | | | Vdc |
| ($V_O$ = 0.5 or 4.5 Vdc) | | 5.0 | 3.5 | – | 3.5 | 2.75 | – | 3.5 | – | |
| ($V_O$ = 1.0 or 9.0 Vdc) | | 10 | 7.0 | – | 7.0 | 5.50 | – | 7.0 | – | |
| ($V_O$ = 1.5 or 13.5 Vdc) | | 15 | 11 | – | 11 | 8.25 | – | 11 | – | |
| Output Drive Current | $I_{OH}$ | | | | | | | | | mAdc |
| ($V_{OH}$ = 2.5 Vdc) Source | | 5.0 | –3.0 | – | –2.4 | –4.2 | – | –1.7 | – | |
| ($V_{OH}$ = 4.6 Vdc) | | 5.0 | –0.64 | – | –0.51 | –0.88 | – | –0.36 | – | |
| ($V_{OH}$ = 9.5 Vdc) | | 10 | –1.6 | – | –1.3 | –2.25 | – | –0.9 | – | |
| ($V_{OH}$ = 13.5 Vdc) | | 15 | –4.2 | – | –3.4 | –8.8 | – | –2.4 | – | |
| ($V_{OL}$ = 0.4 Vdc) Sink | $I_{OL}$ | 5.0 | 0.64 | – | 0.51 | 0.88 | – | 0.36 | – | mAdc |
| ($V_{OL}$ = 0.5 Vdc) | | 10 | 1.6 | – | 1.3 | 2.25 | – | 0.9 | – | |
| ($V_{OL}$ = 1.5 Vdc) | | 15 | 4.2 | – | 3.4 | 8.8 | – | 2.4 | – | |
| Input Current | $I_{in}$ | 15 | – | ±0.1 | – | ±0.00001 | ±0.1 | – | ±1.0 | μAdc |
| Input Capacitance ($V_{in}$ = 0) | $C_{in}$ | – | – | – | – | 5.0 | 7.5 | – | – | pF |
| Quiescent Current (Per Package) | $I_{DD}$ | 5.0 | – | 5.0 | – | 0.005 | 5.0 | – | 150 | μAdc |
| | | 10 | – | 10 | – | 0.010 | 10 | – | 300 | |
| | | 15 | – | 20 | – | 0.015 | 20 | – | 600 | |
| Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) ($C_L$ = 50 pF on all outputs, all buffers switching) | $I_T$ | 5.0 | $I_T = (0.42\ \mu A/kHz)f + I_{DD}$ | | | | | | | μAdc |
| | | 10 | $I_T = (0.85\ \mu A/kHz)f + I_{DD}$ | | | | | | | |
| | | 15 | $I_T = (1.43\ \mu A/kHz)f + I_{DD}$ | | | | | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: $I_T$ is in μA (per package), $C_L$ in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.001.

**SWITCHING CHARACTERISTICS** (Note 5) ($C_L$ = 50 pF, $T_A$ = 25°C)

| Characteristic | Symbol | $V_{DD}$ Vdc | Min | Typ (Note 6) | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise and Fall Time | $t_{TLH}$, | | | | | ns |
| $t_{TLH}$, $t_{THL}$ = (1.5 ns/pF) $C_L$ + 25 ns | $t_{THL}$ | 5.0 | – | 100 | 200 | |
| $t_{TLH}$, $t_{THL}$ = (0.75 ns/pF) $C_L$ + 12.5 ns | | 10 | – | 50 | 100 | |
| $t_{TLH}$, $t_{THL}$ = (0.55 ns/pF) $C_L$ + 9.5 ns | | 15 | – | 40 | 80 | |
| Propagation Delay Time | $t_{PLH}$, | | | | | ns |
| Clock to Q1 | $t_{PHL}$ | | | | | |
| $t_{PHL}$, $t_{PLH}$ = (1.7 ns/pF) $C_L$ + 175 ns | | 5.0 | – | 260 | 520 | |
| $t_{PHL}$, $t_{PLH}$ = (0.66 ns/pF) $C_L$ + 82 ns | | 10 | – | 115 | 230 | |
| $t_{PHL}$, $t_{PLH}$ = (0.5 ns/pF) $C_L$ + 55 ns | | 15 | – | 80 | 160 | |
| Clock to Q14 | | | | | | ns |
| $t_{PHL}$, $t_{PLH}$ – (1.7 ns/pF) $C_L$ + 1735 ns | | 5.0 | – | 1820 | 3900 | |
| $t_{PHL}$, $t_{PLH}$ = (0.66 ns/pF) $C_L$ + 772 ns | | 10 | – | 805 | 1725 | |
| $t_{PHL}$, $t_{PLH}$ = (0.5 ns/pF) $C_L$ + 535 ns | | 15 | – | 560 | 1200 | |
| Propagation Delay Time | $t_{PHL}$ | | | | | ns |
| Reset to $Q_n$ | | | | | | |
| $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 285 ns | | 5.0 | – | 370 | 740 | |
| $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 122 ns | | 10 | – | 155 | 310 | |
| $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 90 ns | | 15 | – | 115 | 230 | |
| Clock Pulse Width | $t_{WH}$ | 5.0 | 500 | 140 | – | ns |
| | | 10 | 165 | 55 | – | |
| | | 15 | 125 | 38 | – | |
| Clock Pulse Frequency | $f_{max}$ | 5.0 | 1.0 | 2.0 | – | MHz |
| | | 10 | 3.0 | 6.0 | – | |
| | | 15 | 4.0 | 8.0 | – | |
| Clock Rise and Fall Time | $t_{TLH}$, $t_{THL}$ | 5.0 | No Limit | | | – |
| | | 10 | | | | |
| | | 15 | | | | |
| Reset Pulse Width | $t_{WL}$ | 5.0 | 3000 | 320 | – | ns |
| | | 10 | 550 | 120 | – | |
| | | 15 | 420 | 80 | – | |
| Reset Recovery Time | $t_{rec}$ | 5.0 | – | 65 | 130 | ns |
| | | 10 | – | 25 | 50 | |
| | | 15 | – | 15 | 30 | |

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

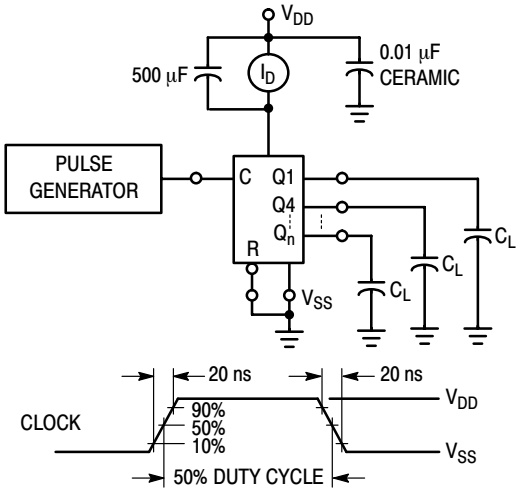



**Figure 1. Power Dissipation Test Circuit and Waveform**

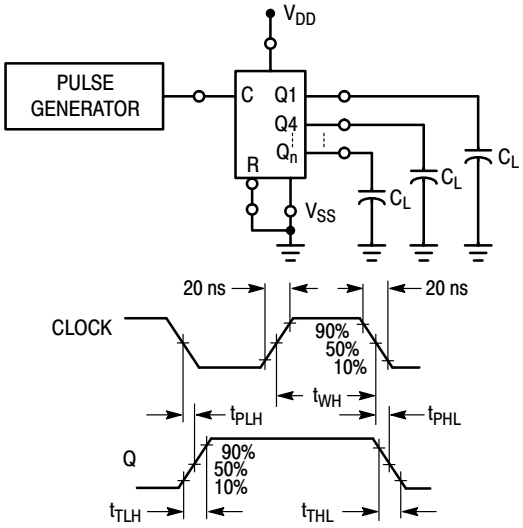



**Figure 2. Switching Time Test Circuit and Waveforms**

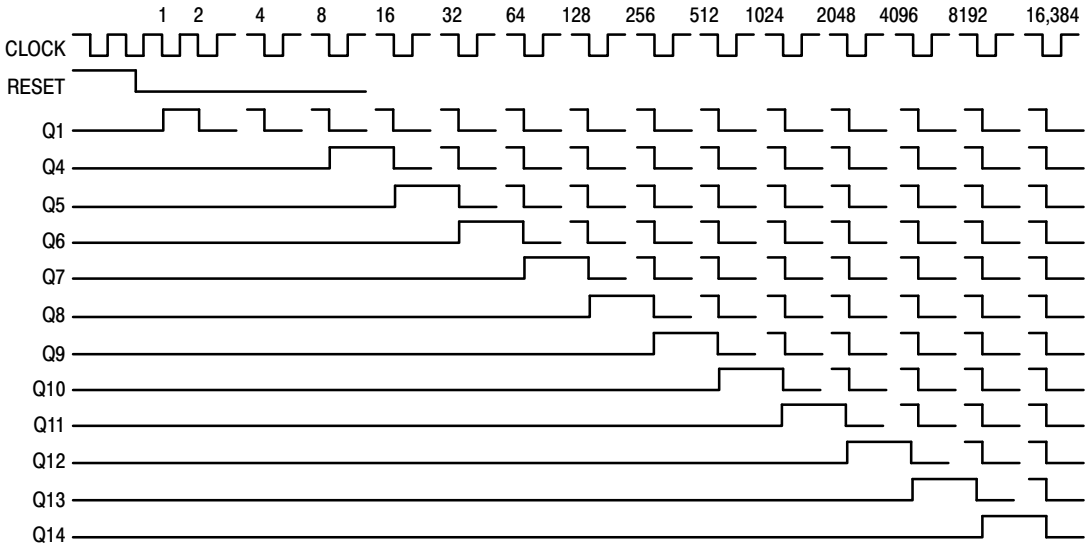
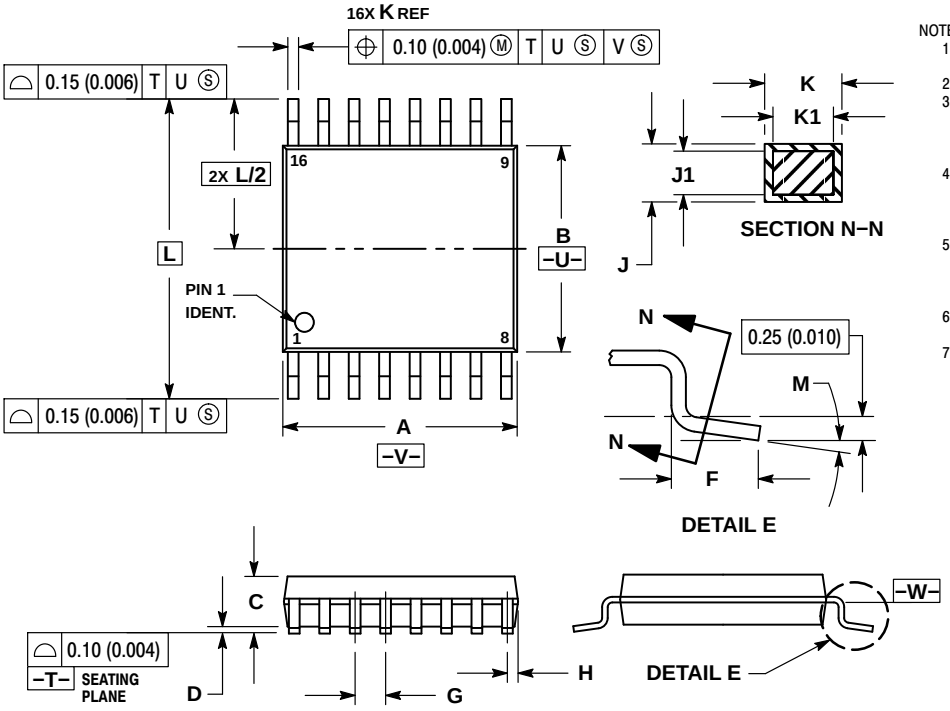



**Figure 3. Timing Diagram**

## PACKAGE DIMENSIONS

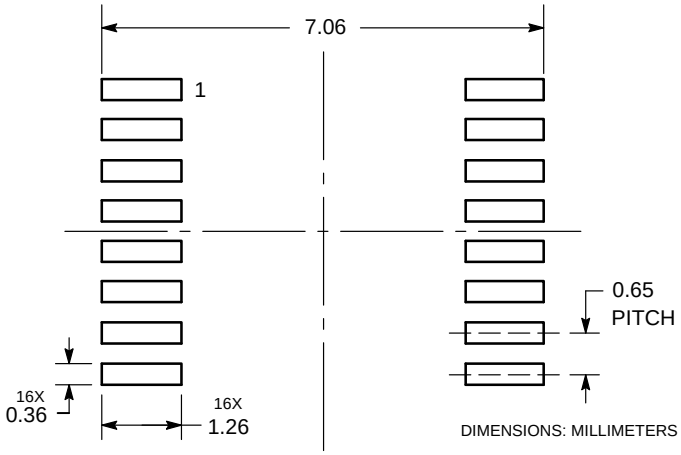
**TSSOP−16**
**DT SUFFIX**
PLASTIC TSSOP PACKAGE
CASE 948F
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

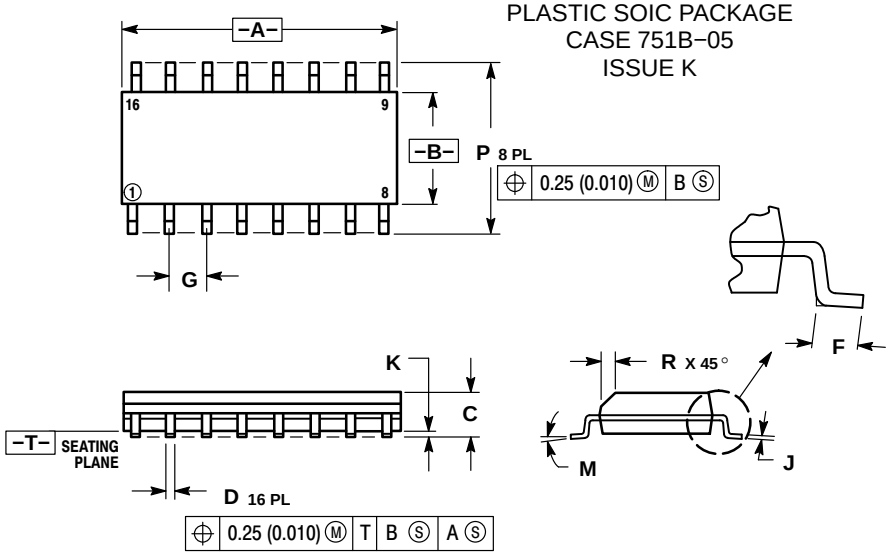
### SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

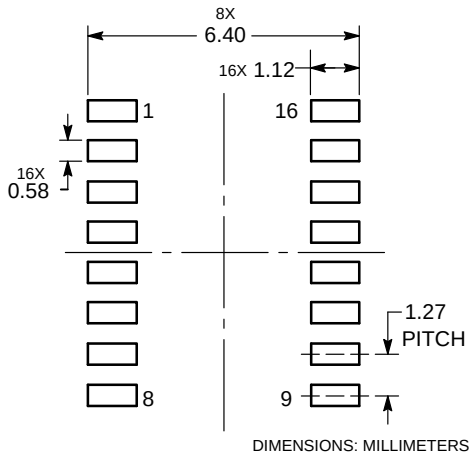
**SOIC−16**
**D SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751B−05
ISSUE K




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

### SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

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